

Today: array multiplier, signed multiply, Booth encoding CO 6.3, 6.

Tomorrow: Booth encoding, fast multipliers CO 6.5

Note: DL 5.6 discusses multiplication as well, I prefer CO

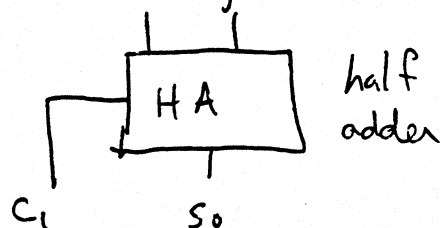
Review (CO 6.1)

grade 1 - add two 1-bit numbers: x_0, y_0

$$\begin{array}{r} x_0 \\ + y_0 \\ \hline C_1 S_0 \end{array}$$

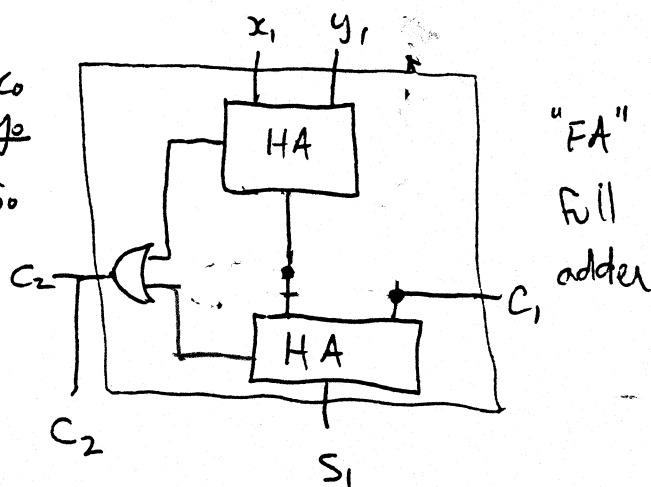
$$S_0 = x_0 \oplus y_0$$

$$C_1 = x_0 \cdot y_0$$



grade 2 - add two 2-bit numbers:

$$\begin{array}{r} C_1 \\ x_1 \ x_0 \\ + y_1 \ y_0 \\ \hline C_2 \ S_1 \ S_0 \end{array}$$



HA and FA add bits of the same magnitude and generate multi-bit result, aka "counter" or "compressor" (bit)

FA is called 3:2 compressor

(3,2) counter

other compressor/counters can be built [advanced multipliers]

grade 3 - multiply two 2-bit numbers
try base 10 first

$$\begin{array}{r}
 13 \\
 \times 11 \\
 \hline
 13 \\
 130 \\
 \hline
 143
 \end{array}$$

multiplicand M
 multiplier Q
 $\leftarrow 13 \times 1$
 $\leftarrow 13 \times 10$
 product P

try binary

$$\begin{array}{r}
 m_1 m_0 \\
 \times q_1 q_0 \\
 \hline
 m_1 q_0 m_0 q_0 \\
 + m_1 q_1 m_0 q_1 \\
 \hline
 \end{array}$$

} form partial products using AND gates
 } sum the partial products, use FA

3rd yr university - multiply in binary, build an array multiplier
(co. 6-3) using digital logic

$$\begin{array}{r}
 1101 \quad (13) \quad M \\
 \times 1011 \quad (11) \quad Q \\
 \hline
 1101 \\
 0000 \\
 1101 \\
 1000 \\
 \hline
 10001111 \quad (143 = 128 + 15) \quad P
 \end{array}$$

array {
 4 bits
 4 bits
 $\downarrow 4+4 =$
 8 bits

- we can build an array structure that adds the partial products as we go from one row to the next
ie, compute new partial products* as a "running total"

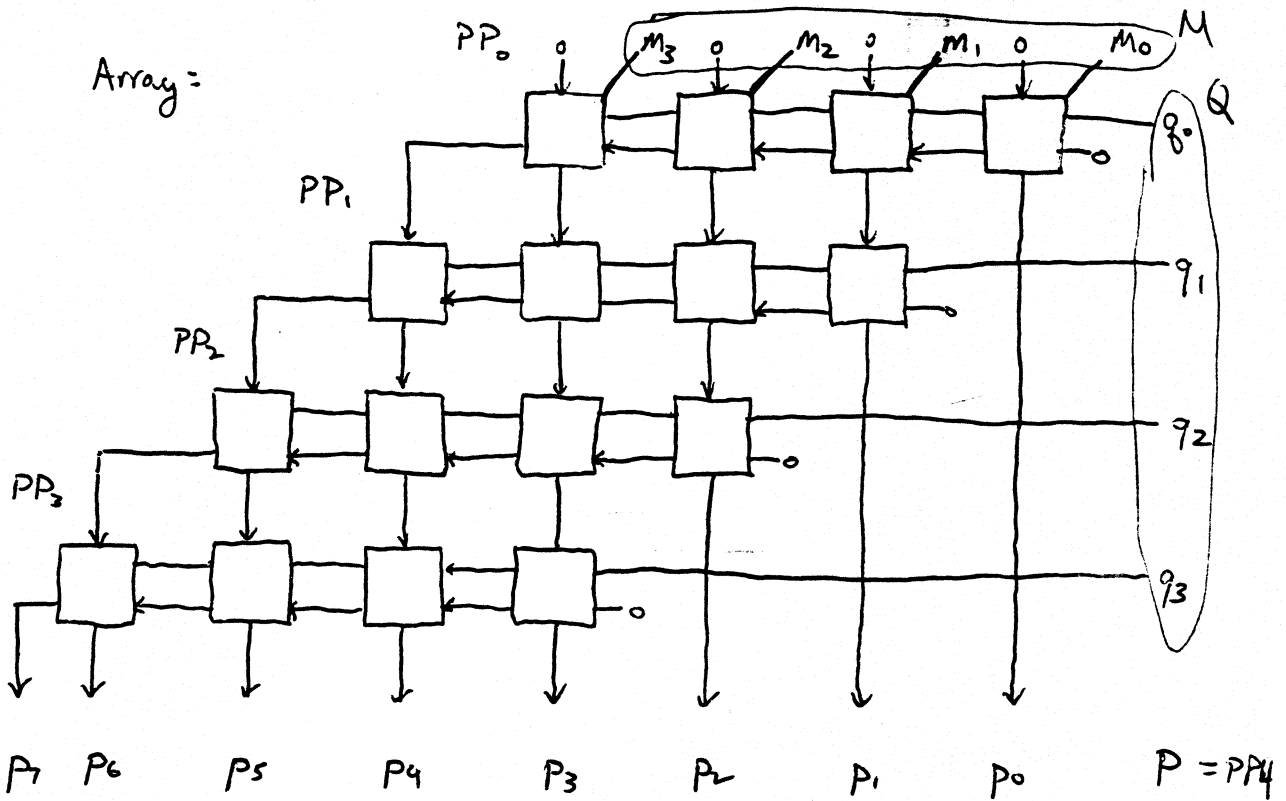
* these are PP_i described in the text

$$\begin{array}{l}
 \text{array "running sum"} \left\{ \begin{array}{l} PP0 \\ PP1 \\ PP2 \\ PP3 \\ PP4 \\ P = PP4 \end{array} \right.
 \end{array}$$

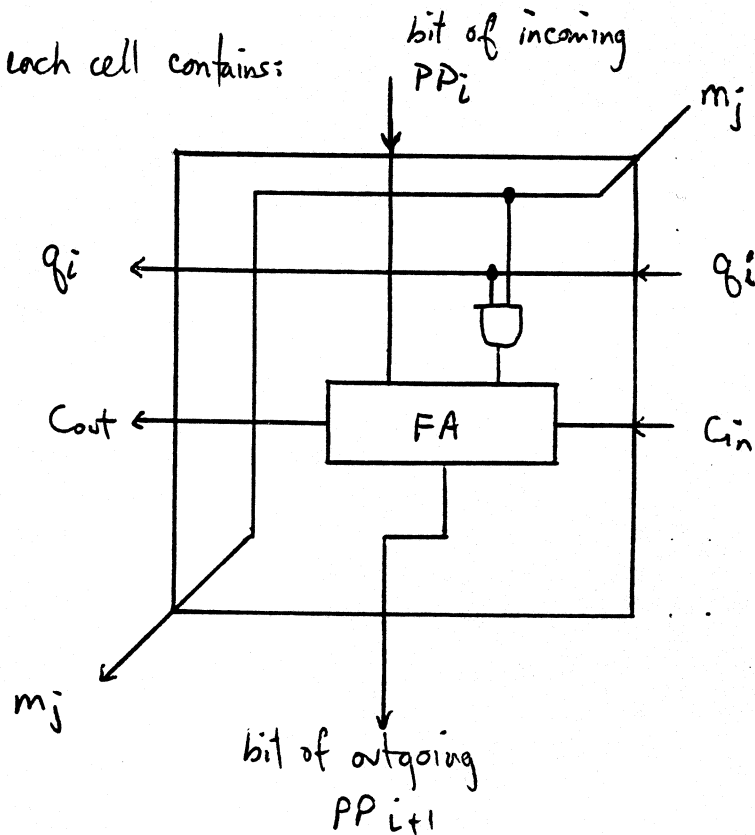
$$\begin{array}{r}
 0000 \\
 1101 \\
 10011 \\
 010011 \\
 1000111 \\
 10001111
 \end{array}$$

$$\begin{array}{r}
 1101 \quad PP1 \\
 + 1101 \\
 \hline
 100111 \quad PP2 \\
 + 0000 \\
 \hline
 100111 \quad PP3 \\
 + 1101 \\
 \hline
 10001111 \quad PP4
 \end{array}$$

Array:



where each cell contains:

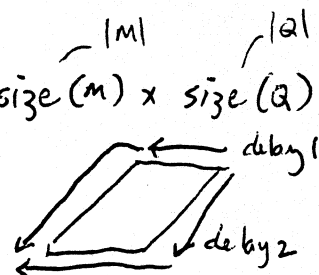


Note: large area (many adders: $\text{size}(m) \times \text{size}(q)$)

worst-case delay roughly $O(|m|) + O(|q|)$

→ we can do better (tomorrow!)

Note: signed numbers? Pair L11



Signed Multiplication (Co 6.4, some new material here not in text)

- Recall: M what if $M < 0$? $Q < 0$?

$$\begin{array}{r} \times Q \\ \hline P \end{array}$$

- We express < 0 numbers in two's complement form: $-M = \bar{M} + 1$

$$\begin{array}{r} 01101 \quad (13) \\ + 00001 \quad (+1) \\ \hline 10011 \quad (-13) \end{array} \quad \begin{array}{r} 10011 \quad (-13) \\ + 00001 \quad (+1) \\ \hline 11011 \quad (13) \end{array}$$

sign bit

- Signed arithmetic uses different logic than unsigned

Rules

Ⓐ if Q unsigned or $Q \geq 0$

multiply by adding sign extension of partial products
→ intuitive (adding signed M 's)

Ⓑ if $Q < 0$

we have two choices:

① note $M \cdot Q = (-M)(-Q) = (\bar{M} + 1)(\bar{Q} + 1)$ +ve, do $Q \geq 0$ case

OR
② use Booth recoding (good, more useful)

Ⓐ sign extension of partial products

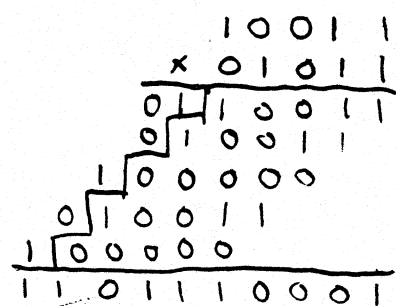
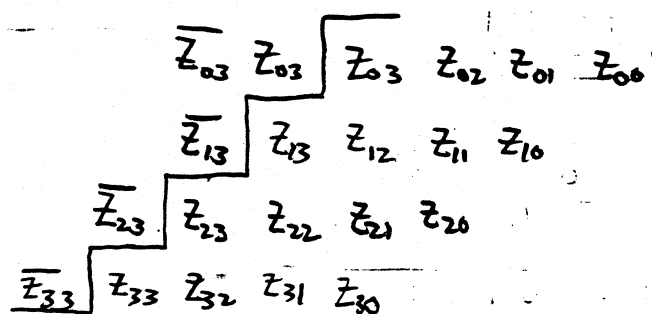
$$\begin{array}{r} 10011 \quad (-13) \\ \times 01011 \quad (+11) \\ \hline 1111110011 \\ 1111100011 \\ 0000000000 \\ 1111000111 \\ 0000000000 \\ \hline 1101110001 \quad (-143) \end{array}$$

Notice: array just got bigger!

Solution 1: D.L. 5.6 shows sign extension by just 1 bit is sufficient if you do running sums of partial products (why?)

Solution 2: not in text...

Sign Extension Optimization (details later)



(-13)

(11)

(-14)

⑧ Booth recoding (to handle $Q < 0$)

- easier than sign extending Q , as well
- useful to build fast multipliers (tomorrow)

we can recode $Q \rightarrow Q'$ using three digits $\{T, 0, 1\}$

$T \equiv -1$ in text

digit q'_i formed by examining $q_i q_{i-1}$:

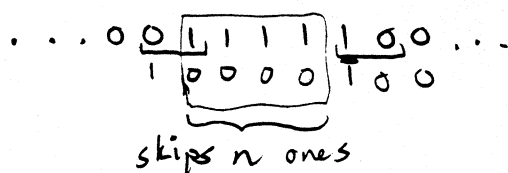
q_i	q_{i-1}	q'_i
0	0	0
0	1	1
1	0	T
1	1	0

assume $q_{-1} = 0$

Example: Q 0 0 1 1 1 0 (30)
 Q' 0 1 0 0 0 T 0 (30, Booth encoded)

Notice: 0 1 0 0 0 T 0 = 0 1 0 0 0 0 0 - 0 0 0 0 0 1 0
 $\uparrow \quad \uparrow$
 $+32 \quad -2 = 0 0 1 1 1 0$
 (32) (2)

often called skipping over 1's:



Now $M \cdot Q = M \cdot Q'$, but we need a new rule for multiplying by Q' (by T in particular)

When we mpy M by $\bar{1}$ ($= -1$), we take the two's complement of M : $\bar{M} + 1$

Example

$$\begin{array}{r}
 \begin{array}{r}
 01101 \quad (13) \\
 \times 11010 \quad (-6) \\
 \hline
 \end{array}
 \rightarrow
 \begin{array}{r}
 \begin{array}{r}
 01101 \\
 \times 01101 \\
 \hline
 1000000 \\
 0100011 \\
 1011011 \\
 0100111 \\
 1000011 \\
 \hline
 1110110010 \quad (-79)
 \end{array}
 \end{array}$$

Note: two's complement
of 13: 10011

Note: each partial product is M , or $-1 * M$, or 0 .

Note: partial products are sign-extended.

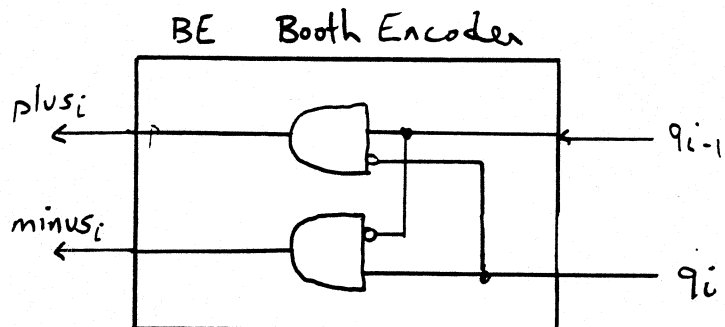
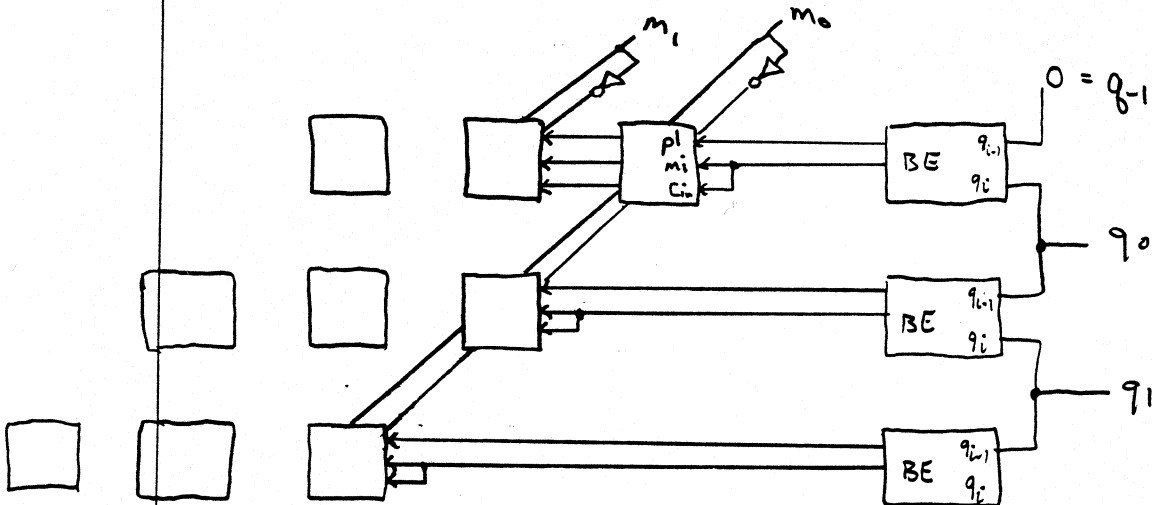
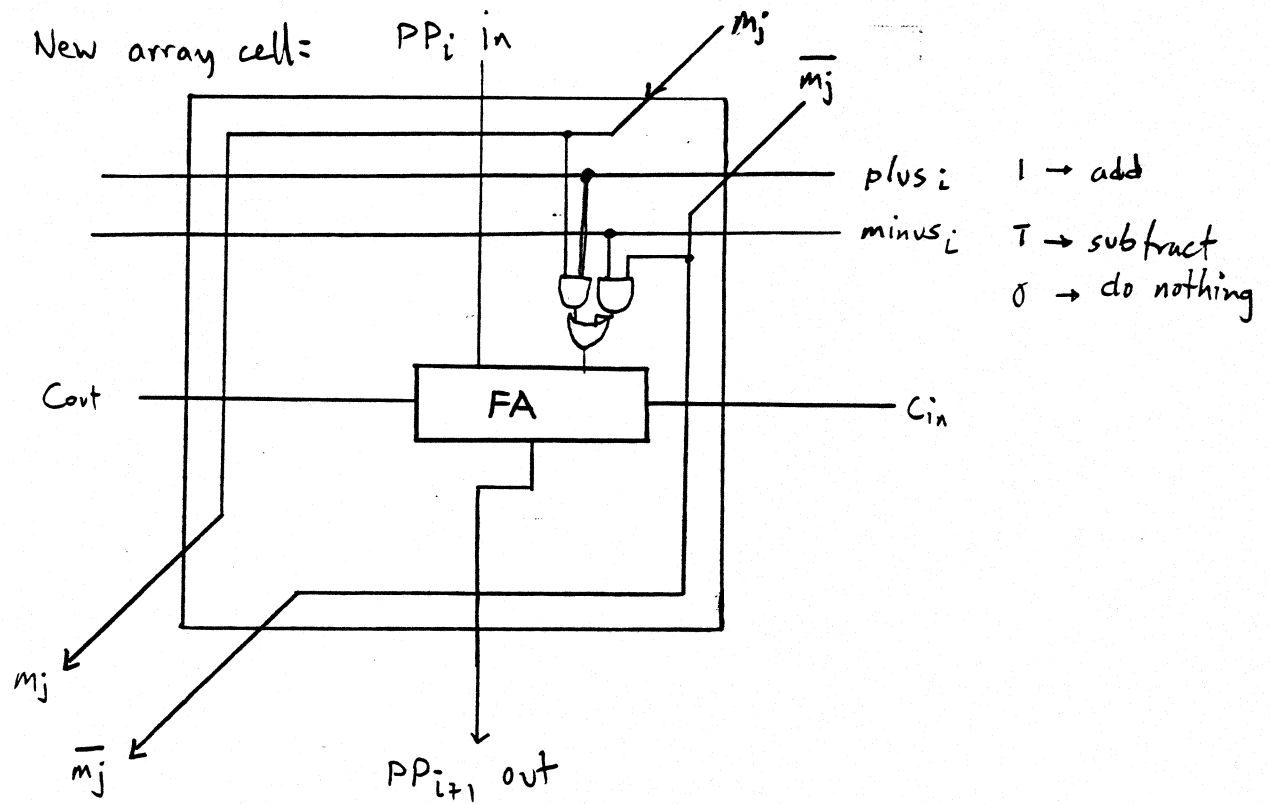
Note: Booth recoding helps us reduce a multiply by a constant to a few shifts and adds. This used to be done by compilers, called "strength reduction", because multiply instructions were very slow (or didn't exist).

Note: $-1 * M = \bar{M} + 1$, but $+1$ is costly (full add!) we can utilize the "carry-in" of the array to get the $+1$ for free!

◦ distribute M , \bar{M} and set C_{in} if using \bar{M}

$$\begin{array}{r}
 Q \quad \begin{array}{r} 11010 \\ \hline 11010 \end{array} \quad (-6) \\
 Q' \quad \begin{array}{r} 0\bar{1}\bar{1}\bar{0} \end{array}
 \end{array}$$

q_i	q_{i-1}	q_i'
0	0	0
0	1	1
1	0	$\bar{1}$
1	1	0



Fast Multiplication (Co 6.5)

- there are many techniques to improve delay and even area of the array multiplier

- look at 2 key techniques:

① Booth recoding in radix-4 (bit-pair recoding)

② carry save addition (Wallace trees)

① Booth recoding in radix-4 (previously, radix 2)

compute Q'' using digits $\{\bar{2}, \bar{1}, 0, 1, 2\}$ as follows:

q_{i+1}	q_i	q_{i-1}	q'_{i+1}	q'_i	q''_i
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	$\bar{1}$	$\bar{1}$
0	1	1	1	0	2
1	0	0	$\bar{1}$	0	$\bar{2}$
1	0	1	$\bar{1}$	1	$\bar{1}$
1	1	0	0	$\bar{1}$	$\bar{1}$
1	1	1	0	0	0

$q_{msb} = \text{sign-extended}$

$q_{-1} = 0$

method:
replace $\begin{matrix} q_{i+1} & q_i \\ \uparrow & \uparrow \\ \text{bit pair} \end{matrix}$ with q''_i

Example $\begin{matrix} \text{sign-ext} & & & & & & \\ \downarrow & & & & & & \\ 1 & 1 & 1 & 0 & 1 & 0 & 0 \end{matrix} \quad (-6)$

$Q' \quad \begin{matrix} 0 & 0 & \bar{1} & 1 & \bar{1} & 0 \end{matrix} \quad (-8 + 4 - 2 = -6)$

$Q'' \quad \begin{matrix} 0 & \bar{1} & \bar{2} \\ \downarrow \times 2^4 & \downarrow \times 2^2 & \downarrow \times 2^0 \end{matrix} \quad (0 - 4 - 2 = -6)$

- To multiply by Q'' , we form partial products $\{\bar{2} * M, \bar{1} * M, 2 * M, M, 0\}$ and add them like before.

- Recall $\bar{2} * M = -2 * M = 2 * (-M) = 2 * (\bar{M} + 1)$
two's complement of M

and $2 * \text{anything}$ is just a shift-left by 1 bit.

Key result: replacing bit-pairs in multiplicand ($Q \rightarrow Q'$) cuts # partial products in half

Block diagram of a Booth's multiplier circuit. The circuit consists of a 4-bit register, a MUX, a Booth Encoder (Booth Enc.), a Full Adder (FA), and a 3-bit register. The 4-bit register has inputs $m_i, \bar{m}_i, m_{i+1}, \bar{m}_{i+1}$ and a zero input. The output of the 4-bit register is connected to the MUX. The output of the MUX is connected to the Booth Encoder. The output of the Booth Encoder is connected to the Full Adder. The output of the Full Adder is connected to the 3-bit register, which has inputs q_{i-1}, q_i, q_{i+1} .

q_i''	max	Cin
1	x_i	0
2	x_{i+1}	0
$\bar{2}$	\bar{x}_{i-1}	1
1	\bar{x}_i	1
0	0	0

shared at right edge of array

Example

Example

sign extension {

									. 0	1	1	0	1
								x	0	-	1	-	2
{	1	1	1	1	1	1	0	0	1	1	0		
	1	1		1	1	0	0	1	1				
	0	0	0	0	0	0							

	1	1	1	0	1	1	0	0	1	0			

(13) 567c

(-6) 5 bits

6 bits

$$\bar{Z} \cdot M = 100110 \text{ bits}$$

$T-M = 110011 \quad 66\frac{2}{3}$

(-78) 10 bits ($= 5 + 5$)

↳ here, we ignored these last bit because operands have only 5 bits \Rightarrow 10 bit product

Example

The diagram shows a horizontal line representing a beam of particles. Above the line are several circles, and below the line are several circles. A wavy line labeled 'B' is positioned below the beam, representing a magnetic field. Arrows indicate the direction of the field and the beam's path.

(13) M

(-11) Q

$$(-16 + 4 + 1 = -11) \quad Q''$$

$M \times Q'' =$

						0	0			0	
					x		I				
0	0	0	0	0	0	0	0		0	0	
0	0	0	0	0	0	0	0		0	0	
1	1	1	1	0	0	1	0		0		
1	1	1	1	0	1	1	0	0	0	0	

optimization: for $\left\{ \begin{array}{l} \bar{z} \cdot M = 2(\bar{M} + 1) \\ 1 \cdot M = \bar{M} + 1 \end{array} \right\}$
use carry-ins for +1

$$\overline{M} + 1$$

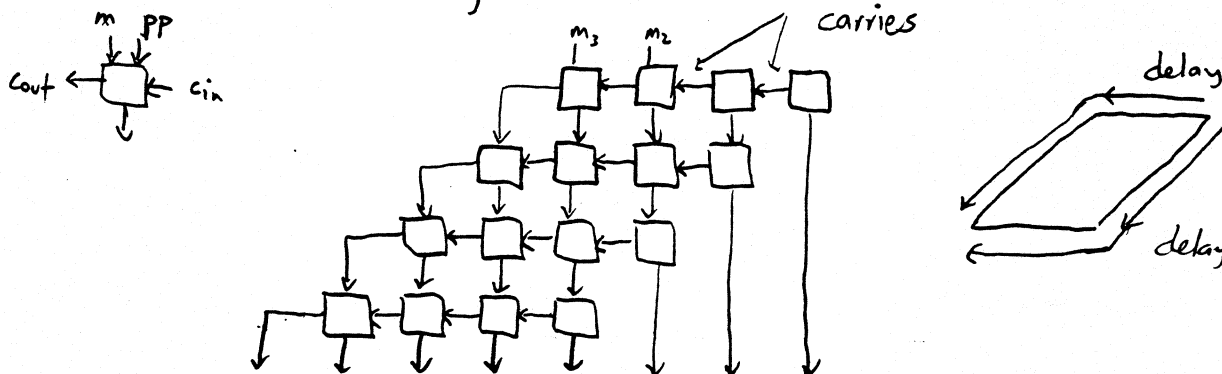
carry-ins

$$(-143) \quad 12\text{-bits } (=6+6)$$

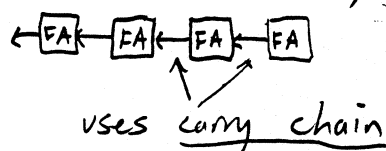
Notice, sign extension is painful again.

② Carry-Save Addition

- consider full array:

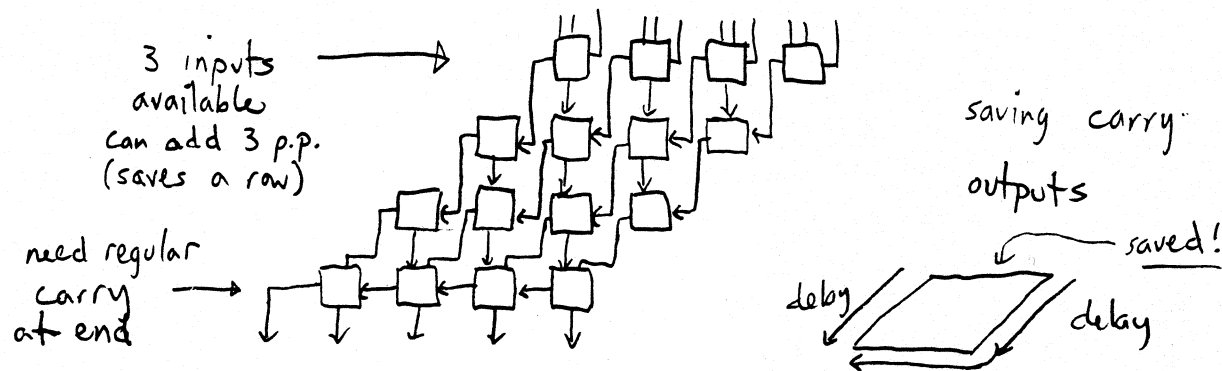


- every row contains a ripple-carry adder:



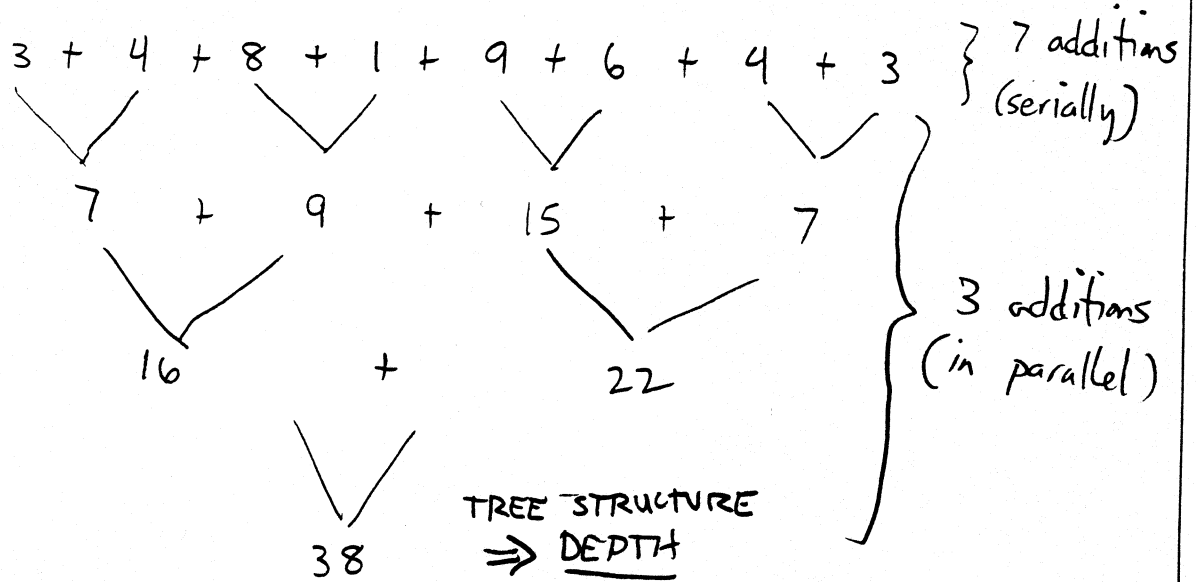
- instead of rippling - left, we can save the carry by sending it downward

note: carry-out is still sent left 1 column, since it has higher weight or magnitude ($\times 2^i$)

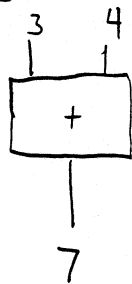


- this saves a bit, but we can do better

How to add 8 numbers quickly?



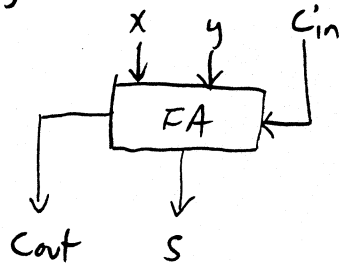
Notice structure:



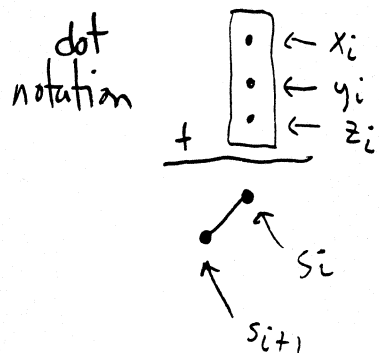
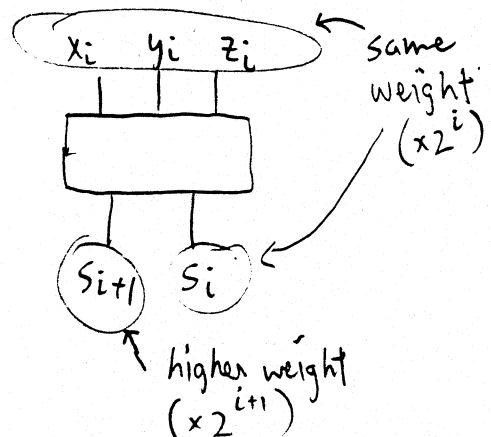
a 2:1
Compressor
(no carry!)



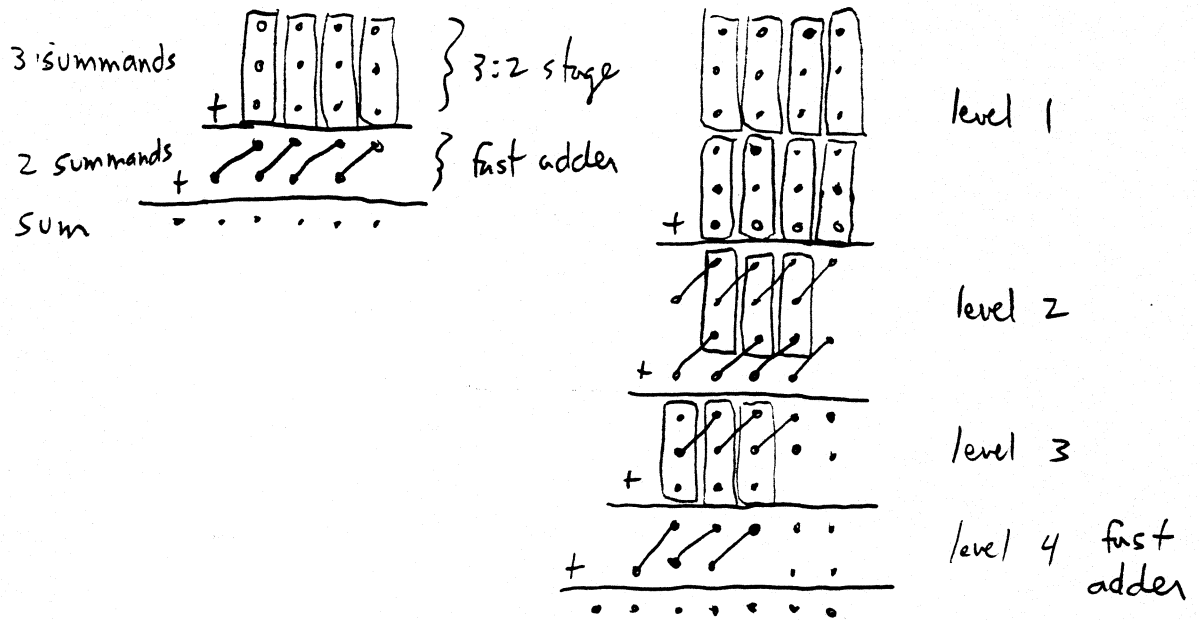
In binary, we have FA, a 3:2 compressor



apply carry-save

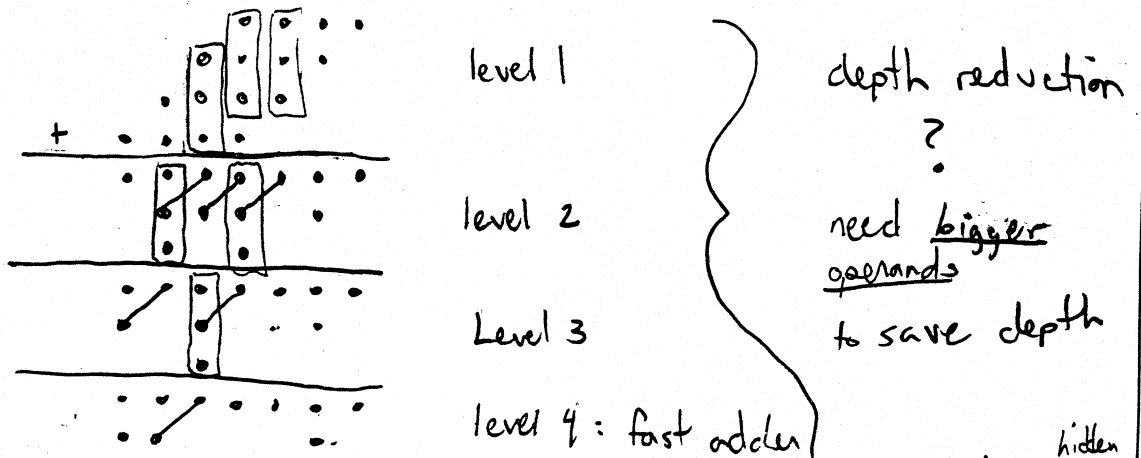


Carry-save addition of 4-bit numbers:

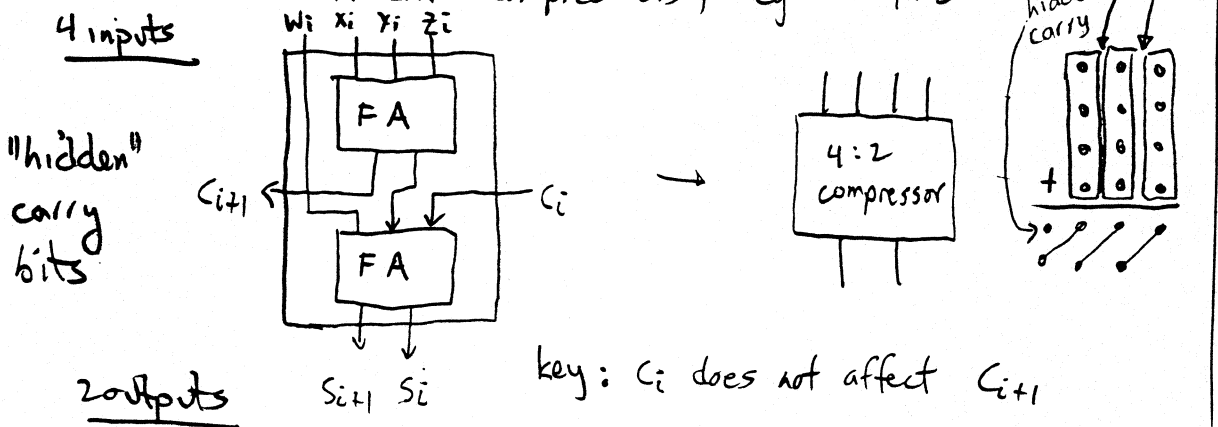


- reduces # levels if adding many #'s : $O(\log n)$
- apply to product term array: WALLACE TREE MULTIPLIER

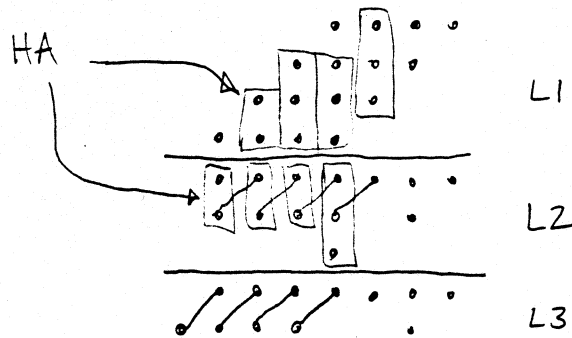
unsigned
4b x 4b
mult:



- can use different compressors, eg: 4:2

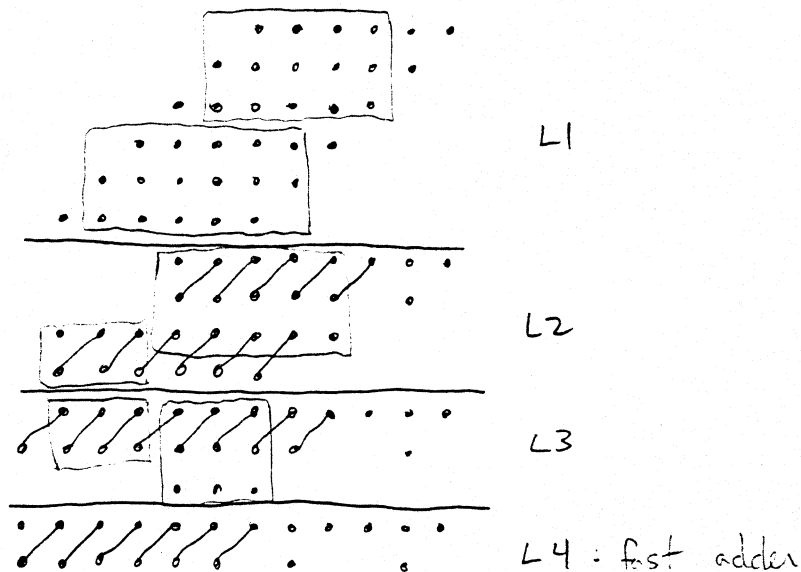


- unsigned 46×46 mult
 - using FA and HA to save one level



note: always use HA to reduce bit pairs on left side

- unsigned 66×66 mult using only 1 more level



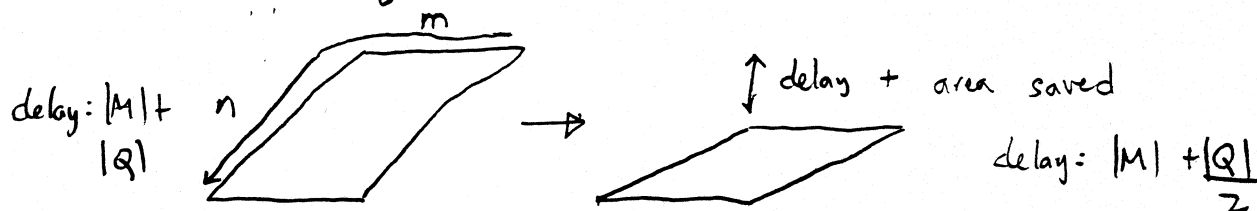
- tree height n levels $\Leftrightarrow \left(\frac{3}{2}\right)^n$ inputs (# partial products)

$$\log_{3/2}(n) \text{ levels} \Leftrightarrow \underbrace{n}_{|Q|} \text{ inputs}$$

- vertical delay $\sim O(\log |Q|)$
- last row : fast adder, horiz. delay $\sim O(\log |M|)$

Summary - Fast Multipliers

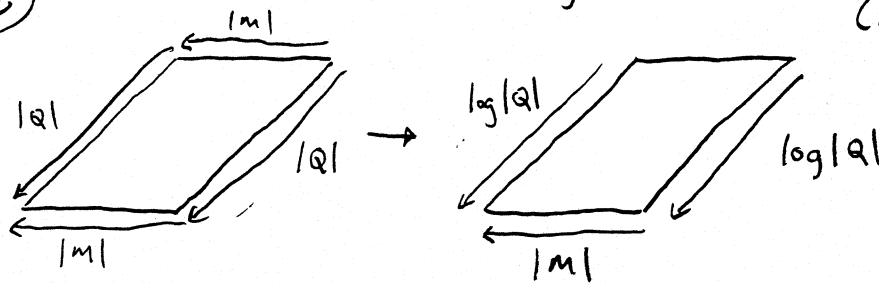
Booth encoding \rightarrow reduce # partial products ($\frac{1}{2}$) w/ radix 4



Carry-save addition (Wallace tree)

tree \rightarrow reduce # levels (effective height) for large # of partial products (vertical delay)

carry-save \rightarrow eliminate ripple-carry in all rows (but last) (horizontal delay)



Fast adder in last row $|M| \rightarrow \log |M|$

final delay $\sim \log |M| + \log |Q|$

compared to $|M| + |Q|$ originally

\rightarrow can combine Booth radix 4 and Wallace

Sign Extension Optimization Details

look carefully at sign extension in the array:

$$\begin{array}{cccc}
 z_{03} & z_{02} & z_{01} & z_{00} \\
 z_{13} & z_{12} & z_{11} & z_{10} \\
 z_{23} & z_{22} & z_{21} & z_{20} \\
 z_{33} & z_{32} & z_{31} & z_{30}
 \end{array}$$

look at left side

$$\begin{array}{cccc}
 z_{03} & z_{02} & z_{01} & z_{00} \\
 z_{13} & z_{12} & z_{11} & z_{10} \\
 z_{23} & z_{22} & z_{21} & z_{20} \\
 z_{33} & z_{32} & z_{31} & z_{30}
 \end{array}
 =
 \begin{array}{cccc}
 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0
 \end{array}
 +
 \begin{array}{cccc}
 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0
 \end{array}$$

new array:

$$\begin{array}{cccc}
 \bar{z}_{03} & z_{02} & z_{01} & z_{00} \\
 \bar{z}_{13} & z_{12} & z_{11} & z_{10} \\
 \bar{z}_{23} & z_{22} & z_{21} & z_{20} \\
 \bar{z}_{33} & z_{32} & z_{31} & z_{30}
 \end{array}$$

ugly to have entire row for just one '1', notice:

$$\begin{array}{r}
 \bar{z}_{03} \\
 + 1 \\
 \hline
 \bar{z}_{03} z_{03}
 \end{array}$$

FINAL ARRAY

$$\begin{array}{cccc}
 \bar{z}_{03} & z_{02} & z_{01} & z_{00} \\
 \bar{z}_{13} & z_{12} & z_{11} & z_{10} \\
 \bar{z}_{23} & z_{22} & z_{21} & z_{20} \\
 \bar{z}_{33} & z_{32} & z_{31} & z_{30}
 \end{array}$$

Example:

$$\begin{array}{r}
 10011 \quad (-13) \\
 \times 01011 \quad (7) \\
 \hline
 0110011 \\
 010011 \\
 000000 \\
 010011 \\
 100000 \\
 \hline
 11011001 \quad (143)
 \end{array}$$

Sign extension optimization w/ Booth radix 4 (optional)

$$\begin{array}{cccccccc}
 z_{06} & z_{06} & z_{06} & z_{06} & z_{06} & z_{06} & z_{05} & \dots & z_{00} \\
 z_{16} & z_{16} & z_{16} & z_{16} & z_{15} & \dots & & & z_{10} \\
 z_{26} & z_{26} & z_{25} & \dots & & & & & z_{20}
 \end{array}$$

↓

$$\begin{array}{cccccc}
 z_{06} & z_{06} & z_{06} & z_{06} & z_{06} & \\
 z_{16} & z_{16} & z_{16} & & & \\
 z_{26} & & & & &
 \end{array}$$

↓

$$\begin{array}{cccc}
 1 & 1 & 1 & 1 \\
 0 & 1 & 0 & 1 & 1
 \end{array}
 +
 \begin{array}{cccc}
 0 & 0 & 0 & 0 & \bar{z}_{06} \\
 0 & 0 & \bar{z}_{16} & & \\
 \bar{z}_{26} & & & &
 \end{array}$$

↓

$$\begin{array}{cccc}
 \bar{z}_{26} & 0 & \bar{z}_{16} & 0 & \bar{z}_{06} \\
 + & 0 & 1 & 0 & 1 & 1 \\
 \hline
 \bar{z}_{26} & 1 & \bar{z}_{16} & 0 & \bar{z}_{06} \\
 + & & & & & &
 \end{array}$$

$$\begin{array}{ccc}
 & & \bar{z}_{06} \\
 + & 1 & 1 \\
 \hline
 \bar{z}_{06} & z_{06} & z_{06}
 \end{array}$$

↓

final array:

sign
extension
still
easy!

$$\begin{array}{cccccccccccc}
 \bar{z}_{06} & z_{06} & z_{06} & z_{06} & z_{05} & z_{04} & z_{03} & z_{02} & z_{01} & z_{00} & C_{00} \\
 | & \bar{z}_{16} & z_{16} & z_{15} & z_{14} & z_{13} & z_{12} & z_{11} & z_{10} & & \\
 \bar{z}_{26} & z_{26} & z_{25} & z_{24} & z_{23} & z_{22} & z_{21} & z_{20} & & & C_{10} \\
 + & & & & & & & & & & C_{26} \\
 \hline
 p_{11} & p_{10} & p_9 & p_8 & p_7 & p_6 & p_5 & p_4 & p_3 & p_2 & p_1 & p_0
 \end{array}$$

Example

[illegible]

(13)

(-11)

1 1 1 1 0 1 1 0 0 0 1

(-143)